IN THE CLAIMS:

Please cancel claims 1-4, 8-11 and 15-16 without prejudice or disclaimer, and amend claims 5-7 and 12-14 as follows:

1-4. (Cancelled)

5. (Currently Amended) [[The]] A disk array device ~~according to claim 3~~ comprising:

a plurality of hard disk drives;

a plurality of channel control units for performing data transfer and reception between the channel control units and a plurality of information processing apparatuses being communicably connected thereto through a storage area network;

a plurality of disk control units for performing data transfer and reception between the disk control units and said plurality of hard disk drives as communicably connected thereto;

a CPU for performing control of said plurality of channel control units and said plurality of disk control units;

a cache memory for storage of data being transferred and received between said channel control units and said disk control units; and

a data transfer integrated circuit communicably connected via more than one bus to said channel control units, said disk control units and said CPU and also connected via a plurality of data buses to said cache memory, wherein

said data transfer integrated circuit is responsive to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using one or more of said plurality of data buses, a number of which is determined in accordance with a transfer data length being set in the access request,

said data buses are two data buses,

said data transfer integrated circuit uses said two data buses to provide access to said cache memory when the transfer data length being set in the access request is

longer than a predefined reference data length and, when the transfer data length set in the access request is shorter than or equal to said predefined reference data length, uses one of said data buses to get access to said cache memory,

said data transfer integrated circuit includes a priority adding unit for adding, when receiving access requests to said cache memory from a plurality of ones of said channel control units or said disk control units or said CPU, an order of priority to the plurality of access requests, and

said data transfer integrated circuit uses said two data buses to provide access to said cache memory when a transfer data length being set in one of said access requests with the highest order of priority is longer than said predefined reference data length and, when transfer data lengths being set in said access request with the highest order of priority and an access request with the second highest order of priority are shorter than said predefined reference data length, said data transfer integrated circuit uses one of said data buses for each of the access requests to thereby get access to said cache memory.

6. (Currently Amended) The disk array device according to claim 5, wherein in case the transfer data lengths being set in said access request with the highest order of priority and said access request with the second highest order of priority are shorter than said predefined reference data length, and when both of said two data buses are idle ~~out of use~~, said data transfer integrated circuit allocates one of said data buses to each of the two access requests and then performs access to said cache memory in a parallel way.

7. (Currently Amended) The disk array device according to claim 5, wherein in case the transfer data length being set in said access request with the highest order of priority is longer than said predefined reference data length, and when any one of said two data buses is busy ~~in use~~, said data transfer integrated circuit allocates a remaining one of said data buses which is out of use with respect to the access request and then

performs access to said cache memory.

8-11. (Cancelled)

12. (Currently Amended) ~~The disk array device~~ A control method ~~according to claim 10~~ of a disk array device arranged to include:

a plurality of channel control units for performing data transfer and reception between the channel control units and a plurality of information processing apparatuses being communicably connected thereto through a storage area network;

a plurality of disk control units for performing data transfer and reception between the disk control units and a plurality of hard disk drives as communicably connected thereto;

a CPU for performing control of said plurality of channel control units and said plurality of disk control units;

a cache memory for storage of data being transferred and received between said channel control units and said disk control units; and

a data transfer integrated circuit communicably connected via more than one bus to said channel control units, said disk control units and said CPU and also connected via a plurality of data buses to said cache memory,

wherein an operation in said data transfer integrated circuit includes the steps of:

receiving an access request to said cache memory from any one of said channel control units, said disk control units and said CPU;

selecting certain one or ones of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request;

using the selected data bus to thereby provide access to said cache memory,

wherein said data buses are two data buses, and

said step of selecting the data buses includes one of the steps of:

selecting said two data buses when the transfer data length being set in the access request is longer than a predefined reference data length; and

selecting one of said data buses when the transfer data length as set in the access request is shorter than or equal to said predefined reference data length,

wherein said data transfer integrated circuit has a step of adding, when receiving access requests to said cache memory from a plurality of ones of said channel control units or said disk control units or said CPU, an order of priority to the plurality of access requests, and

said step of selecting the data buses includes one of the steps of:

selecting said two data buses when a transfer data length being set in one of said access requests with the highest order of priority is longer than said predefined reference data length, and

when transfer data lengths being set in said access request with the highest order of priority and an access request with the second highest order of priority are shorter than said predefined reference data length, selecting one of said data buses for each of the access requests.

13. (Currently Amended) The disk array device control method according to claim 12, wherein in an event that the transfer data lengths being set in said access request with the highest order of priority and said access request with the second highest order of priority are shorter than said predefined reference data length, and when both of said two data buses are idle ~~out of use~~, said step of selecting the data buses selects one of said data buses to each of the two access requests.

14. (Currently Amended) The disk array device control method according to claim 12, wherein in case the transfer data length being set in said access request with the highest order of priority is longer than said predefined reference data length, and when any one of said two data buses is busy ~~in use~~, said step of selecting the data

buses selects a remaining one of said data buses which is out of use with respect to the access request.

15-16. (Cancelled)